ABSTRACT

A method for detecting a phase difference between an input clock signal and a feedback output clock signal, correcting by delaying time corresponding to the phase difference, and generating a phase control signal delayed for a time period corresponding to the phase difference is disclosed.

A 50% duty factor is sustained by delaying the phase control signals delayed for a period time corresponding to the phase difference for a predetermined period of time. In this case, the preset time is set to compensate a delayed time of the circuit element whereby the phase control signal passes.